ABSTRACT

A content addressable memory is implemented as a memory with a L-level hierarchy. When accessing the memory, key data is compared at each level of the hierarchy to determine whether an exact match, a longest prefix match exists. The CAM may be implemented with a two level hierarchy and a memory configuration that stores keys in cyclical ascending or cyclical descending order. Each memory row may include row logic to create the first level hierarchical data directly from its row data. The row data itself comprises the second level hierarchical data. During the search process, the key data is compared to the first level hierarchical data which narrows the search to only particular memory rows for the exact match or longest prefix match operation. This architecture is fast, power efficient and makes efficient use of transistors. Additional row logic and a dual port memory implementation permits the insertion and deletion of key elements into and from rows in a single parallel operation that maintains the cyclical ascending or descending order of key elements in the rows rather than multiple operations.